ECE SPARK 2026

Opto-isolated Gate Driver for sub-10ns GaN HEMT

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Objective

What are you trying to accomplish?

- Implement ultra-fast, optically isolated gate drive for bare-die GaN & SiC FETs
- Eliminate driver ICs using bare-die photovoltaic (PV) cell & CoB phototransistor to switch 300V–3300V at 1 MHz with sub-10 ns transitions

Why is this objective important?

- Rapid transitions cause severe EMI & noise that corrupts signals
- Optical isolation offers total EMI immunity, zero parasitic capacitance, & high voltage safety
- Enables highly efficient power conversion in LiDAR, data centers, and wireless charging

What is the definition of success?

- Achieving sub-10 ns V_{DS} rise/fall times during Double Pulse Test (DPT) without false triggering or LC ringing

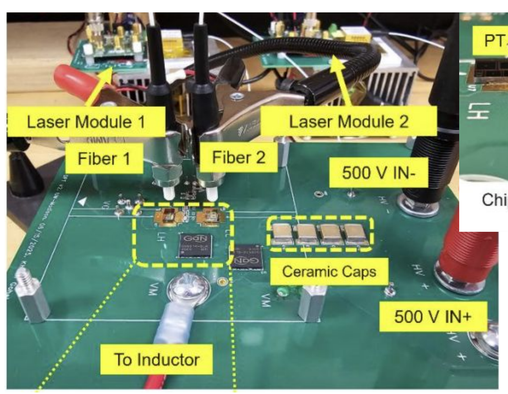
Background

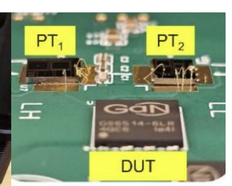
Previous solutions & alternatives:

- **Standard Electrical Drivers (Galvanic/Magnetic):**
  - **Pros:** High peak current, fast response
  - **Cons:** Parasitic capacitance degrades signal, induces noise
- **Commercial Integrated Optocouplers (FOD8384):**
  - **Pros:** Integrated, easy to implement
  - **Cons:** Slow rise/fall (57.6/34.5 ns), gate ringing
- **Directly Optically Triggered GaN HEMTs:**
  - **Pros:** Eliminates gate driver stage entirely
  - **Cons:** Low photocurrent, threshold drift, sluggish switching

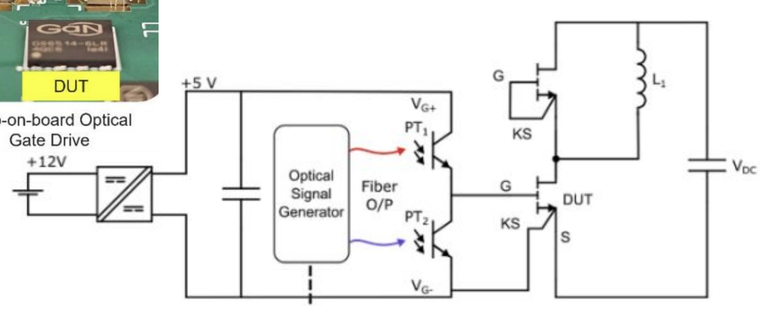
The CoB-PT Architecture (Wide-Bandgap Transistor Group):

- Achieves V_{DS} rise/fall times of under 10 ns for 300-3300V
- >7× faster than prior optical control via state-of-the-art electrical gate drivers
- Total optical EMI immunity & 3 kV+ galvanic isolation





Chip-on-board Optical Gate Drive



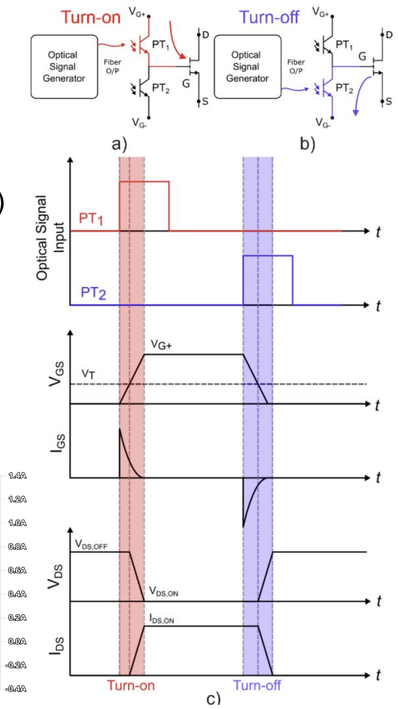
Approach / Methodology

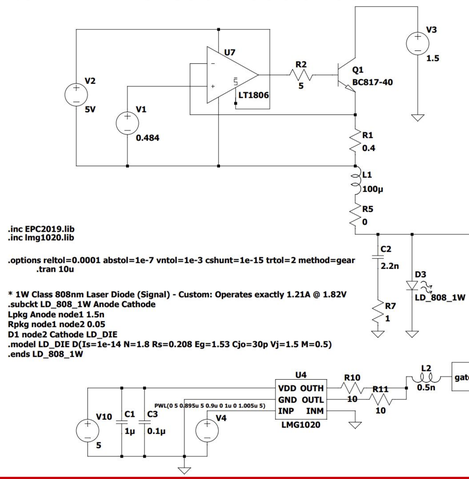
System Architecture & What Was Done:

- **Optical Transmitter:** 2-channel function generator provides pulses to a custom laser driver powering 808 nm laser diodes and third LED provides optical power to PV cell
- **Discrete CoB Totem-Pole Receiver:** Mounted bare GaAs NPN phototransistor dies (PT1 pull-up, PT2 pull-down) directly on the PCB right next to the GaNFET gate

Methodology for Trustworthy Results:

- **SPICE Modeling:** Behavioral models of GaAs phototransistors; parasitics included (0.5–2 nH).
- **Double Pulse Test (DPT):** Validated switching speeds; large load inductance ensures first-pulse quality.
- **Probing:** On-board SMA (V_{GS}) & 500 MHz passive probe (V_{DS}) to minimize lead inductance.





SPICE model of voltage controlled current source powering an 808nm laser

Results and Conclusions

What was completed?

- Re-engineered schematics for discrete CoB totem-pole in LTSpice
- Designed laser driver board & finalized component selection (PCB fabrication pending)
- Selected gate driver components and analyzed GaN/SiC FETs using Figures of Merit (FOM)

What remains to be completed?

- Assemble dual-PCB stacked architecture with laser driver suspended approx 10 mm above gate driver board
- Integrate bare-die PV cell powered by 650 nm (red) LED to eliminate DC-DC converter, ensuring 100% optical power and total electromagnetic isolation